ALBERT L. ALUMNUS

12 Washington Street Santa Clara, CA 95052 (408) 554-4421 albertalumnus@xxxx.com

SUMMARY:

- Hardware engineer with 10+ years IC design experience and a proven track record of meeting deadlines
- Experienced project team lead, customer interface, and team player
- Front-to-back design experience for analog and digital ICs, including transistor-level design, physical design, and timing closure
- Expertise in Design-for-Test methodologies and implementation
- Granted patent for Built-in-Test architecture

TOOLS:

- **Analog:** Analog Design Environment Suite: Composer, Virtuoso, Assura
- **RF**: ADS, Spectre-RF
- **Digital:** Silicon Ensemble, Design Compiler, PrimeTime, Verilog-XL
- **Languages:** PERL, Verilog, OCEAN

EXPERIENCE:

IC Design Engineer, ABC Technologies Inc.,San Jose, CA June 20xx to Present

- Design and develop analog CMOS controller circuits for leveling the power amplifier output in GSM phone platforms. Architecture includes a high-speed LDO and a closed-loop controller for polar-EDGE platform
- Design PA bias-control IC for a linear-EDGE front-end module (FEM)
- Execute co-simulation of GaAs power amplifier and CMOS controller to debug and repair power-up transient problems
- Create floor plan and full-custom layout of CMOS IC, achieving size/cost target
- Perform top-level integration and verification, hitting target tape-out schedule for each product
- Design IC test plan, hardware schematic, and assist in debug
- Circuits include: Op Amps, Bandgap Reference, V-to-I Converter, Sample-and-Hold

Hardware Design Engineer, XYZ Inc**.,** San Jose, CA June 20xx to June 20xx

- Invented built-in-test methodology for pulse-width modulator driving the laser, which dramatically increased fault coverage and significantly reduced test time
- Ported PLL (VCO, charge-pump, pre-charge circuit) from 0.25um to 0.18um process, reducing time-to-market and earning recognition award
- Designed JPEG-encoder memory interface, in Verilog, for new product
- Created floorplan and routed formatter IC for the C800 high-end product
- Performed static-timing analysis and timing closure on B200 formatter IC
- Executed design-for-test checks, modified as needed, and ensured target fault coverage
- Integrated top-level and supervised mask designer on delta-sigma ADC test chip
- Mentored and trained multiple junior engineers and summer students in our design flow

Test Development Engineer, DEF Co., IC Division**,** San Jose, CA July 20xx to June 20xx

- Design and develop production-quality test hardware and software for high-speed bipolar analog and mixed-signal integrated circuits and transferring both into production.
- Wrote time-efficient test program for 1GHz dual-channel 54-to-2 analog MUX
- Designed test hardware for 4GHz 8-channel logic analyzer acquisition IC
- Inherited hardware, completed software, and transferred into production the test for a
- 500MHz single-shot 2GS/s 8-bit flash ADC

EDUCATION:

M.S. in Electrical Engineering, **Stanford University** Palo Alto, CA
B.S. in Electrical Engineering, **Santa Clara University** Santa Clara, CA

OTHER:

- U.S. Patent 6,xxx,xxx: Method for Delay Line Linearity Testing
- Received special contributor achievement award for ABC product lines, presented by the customer
- IEEE Senior Member
- Campus Manager for ABC recruiting at SCU