High-Frequency On-Chip Inductance Model

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***Abstract*—The effect of random signal lines on the on-chip inductance is quantitatively investigated, using an S-parameter-based methodology and a full wave solver, leading to an empirical model for high-frequency inductance. The results clearly indicate that the random signal lines as well as designated ground lines provide return paths for gigahertz-frequency signals. In particular, quasi TEM-wave-like propagation mode is observed above 10 GHz, revealing a unique relationship between capacitance and inductance of the signal line. Incorporating the random capacitive coupling effect, our frequency-dependent *RLC* model is confirmed to be valid up to 100 GHz.**

***Index Terms*—Electromagnetic coupling, high-speed integrated circuits, inductance, integrated circuit interconnections, modeling.**

I. Introduction

With relentless pursuit of Moore's law toward faster and larger ULSI systems, on-chip inductance has emerged as an imperative design consideration. But modeling and extraction of on-chip inductance are not as straightforward as their capacitance counterparts due to long-range interaction of the magnetic field and unknown return paths. In a typical on-chip interconnect configuration shown in Fig. 1, power lines provide good return paths at low frequencies. As the frequency of the signal advances into multi-gigahertz regime, however, virtually all the wires surrounding the signal line should be considered as possible return paths. Recently Kleveland [1] showed experimentally that random signal lines reduce high-frequency inductance significantly by providing closer return paths through capacitive coupling. As the signal frequency continues to increase, the random capacitive coupling phenomenon becomes more dominant. Nevertheless, there has been no quantitative analysis on the phenomenon. In this Letter, we investigate quantitatively the effect of random signal lines on the high-frequency inductance using a full wave solver [2], and for the first time, we present a frequency-dependent *RLC* model valid up to 100 GHz.

II. Experimental Methodology

Our test structures are designed to resemble a typical interconnect configuration (see Fig. 1) in high-performance digital chips. A signal line, running between parallel ground lines simulating power lines in a real chip, is surrounded by additional random parallel lines in the same layer of the signal line and random crossing lines in adjacent layers. Since the random lines provide return paths only via displacement current, they are left floating.[1] The width, space, and density of parallel and crossing random lines are varied to demonstrate the effect of the random lines on the inductance of the signal line. Telegrapher's parameters (RLCG) for each structure are extracted from the S-parameters obtained using a full wave solver [2] for frequencies

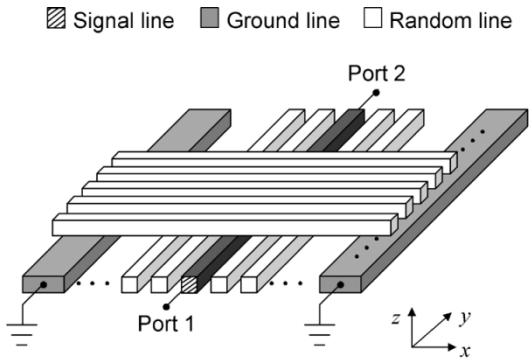

Fig. 1. Test structure used to extract telegrapher's parameters (RLCG) and investigate the high-frequency behavior of on-chip inductance. Geometry of the random lines such as length, width, spacing, and density is varied. The dimensions of the structure are not drawn to scale. The telegrapher's parameters do not depend on the length of the structure. Wires are assumed to be copper with a conductivity of 5.8×10^7 Siemens/meter and an intermetal dielectric constant of 2.9 is used.

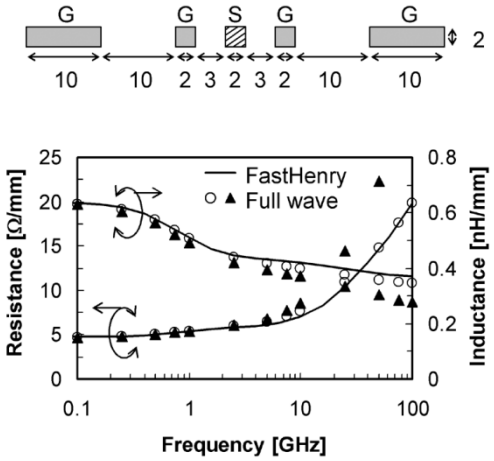

Fig. 2. Resistance and inductance extracted using quasistatic [3] and full wave [2] solvers for a structure shown above. Numbers in the structure represent dimensions of the structure in micrometers. In the full wave method, the basic structure (circle) and a structure with floating random parallel and crossing lines (triangle) are extracted, while only the basic structure (line) is extracted in the quasi-static method for comparison purposes.

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[1]Here we neglect finite admittances of driver and load for each random line. In [1], the authors show that a bias on the gate drivers of the random lines has minor effects on inductance extraction results, supporting our assumption.

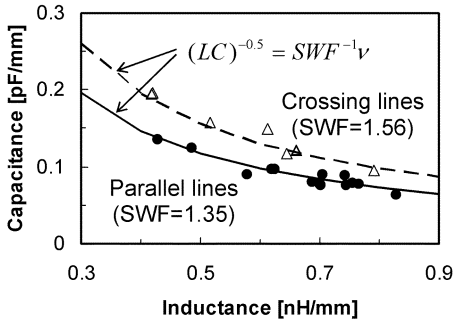

Fig. 3. Relationship between capacitance and inductance extracted at 20.1 GHz for various capacitive coupling configurations. Lines represent the fitted slow-wave mode relationship as indicated, where SWF and v are slow-wave factor and phase velocity in the medium of the structure, respectively.

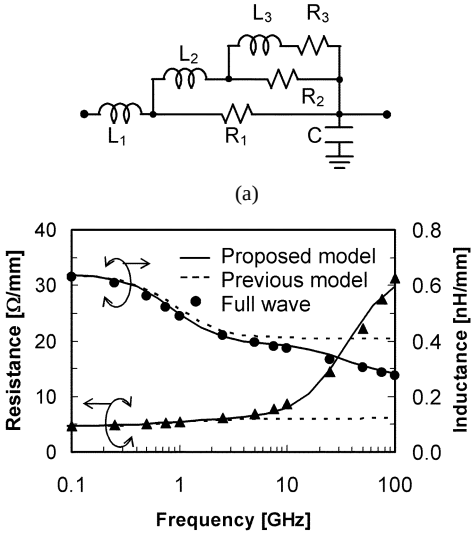

Fig. 4. (a) Frequency-dependent lumped *RLC* model and (b) comparison with full wave solver. The structure in Fig. 2 with random signal lines is used to extract physical parameters, from which values of the lumped elements can be computed. In (b), the extracted L and R are compared with results from a full wave solver and a previous model [5].

ranging from 100 MHz to 100 GHz. In Fig. 2, the extracted R and L for a given structure are shown. For comparison, parameters directly obtained from a quasi-static 3-D inductance extractor, FastHenry [3], are also shown. The excellent match between the two solvers for the basic structure validates our parameter extraction methodology. In Fig. 2, the switch of return path from the wide and far ground lines to the thin and close ground lines is manifested in the change in resistance and inductance with frequency. Between 10 and 100 GHz, inductance decreases more rapidly, while resistance increases exponentially due to skin effect. By adding random coupling lines to the basic structure, we observe further reduction of inductance and increase of resistance for frequencies above 10 GHz, indicating the participation of the random lines as return paths.

III. Model Construction and Discussion

Since the random lines participate as return paths through capacitive coupling, the relationship between the high-frequency inductance and capacitance of the signal line is examined. At high frequencies, the inclusion of parallel random signal lines suggests quasi TEM-mode wave propagation by providing pseudo ground lines next to the signal line. This hypothesis is supported by the close correlation between L and C as shown in Fig. 3, where the L and C parameters extracted for various interconnect configurations are plotted together. Based on transmission line theory, the reciprocal of the LC product for TEM wave being the square of the phase velocity, our simulation data are fitted to a semi-empirical expression

$$(LC)^{-0.5} = SWF^{-1}\nu \tag{1}$$

where ν is the phase velocity in the medium and SWF is the dimensionless "slow-wave factor" used to characterize the deviation from ideal wave propagation along a standard transmission line. In Fig. 3, crossing random coupling lines show a slightly slower wave-like propagation mode than parallel lines, as the former can support electric field more easily than magnetic field. By introducing separate SWFs for parallel and crossing lines, which depend on the technology, the high-frequency inductance can be extracted from the parasitic capacitance [4] of the signal line using (1). Since both parallel and crossing lines exist in a real chip, final inductance value is calculated from a parallel combination of inductances due to parallel lines and crossing lines, respectively.

In Fig. 4(a), we use parallel branches to model frequency dependency of R and L, as in Krauter [5]. The values of the lumped elements in the model can be calculated from the following six extracted physical parameters for any interconnect structure:

$$\begin{aligned}
&R_{\mathrm{DC}} = R_1 \| R_2 \| R_3 \\
&L_{\mathrm{DC}} = L_1 + \left(\frac{R_1}{R_1 + R_2 \| R_3}\right)^2 \left(L_2 + \left(\frac{R_2}{R_2 + R_3}\right)^2 L_3\right) \\
&R_{\mathrm{MF}} = R_1 \| R_2; \qquad L_{\mathrm{MF}} = L_1 + \left(\frac{R_1}{R_1 + R_2}\right)^2 L_2 \\
&R_{\mathrm{HF}} = R_1; \qquad L_{\mathrm{HF}} = L_1.
\end{aligned} \tag{2}$$

The low-frequency (DC) and moderate-frequency (MF) parameters, R_{DC}, L_{DC}, R_{MF}, and L_{MF} are extracted analytically from the configuration of the signal line and designated ground lines [6]. High-frequency inductance (L_{HF}) is extracted from the parasitic capacitance using (1). We use the modified skin-effect formula proposed by Kleveland [1] to extract high-frequency resistance (R_{HF}). In Fig. 4(b), our model is compared with Krauter's [5] as well as with a full wave solver. Our model shows excellent match for a wide range of frequencies, from 100 MHz to 100 GHz, while the other significantly overestimates high-frequency inductance and considerably underestimates high-frequency resistance. Furthermore, by increasing extraction frequency from 20.1 to 100 GHz, we have found that the SWF changes by only 13%. Therefore, a single SWF can be used up to 100 GHz, although SWF is slightly frequency-dependent, approaching unity at infinite frequency.

IV. Summary

The effect of random signal lines on high-frequency on-chip inductance is quantitatively investigated. Using a full wave

solver and S-parameter-based methodology, quasi-TEM mode wave propagation through the random lines is observed above 10 GHz, revealing a unique relationship between capacitance and inductance of the signal line. From this relationship, we extract high-frequency inductance analytically from the parasitic capacitance. Having incorporated random capacitive coupling and skin effects, our frequency-dependent *RLC* model is confirmed to be valid up to 100 GHz.

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