Characteristics of Aligned Carbon Nanofibers for Interconnect Via Applications

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***Abstract*—Electrical properties of plasma-enhanced chemical vapor deposited carbon nanofibers (CNFs) are characterized with measurements over a broad temperature range (4–300 K). Temperature-dependent measurements of CNF via resistivity reveal a behavior resembling the mixture of graphite a-axis and c-axis transport mechanisms. For the first time, temperature-dependent characteristics of CNFs are measured and modeled based on previously developed models for electron conduction in graphite. Reliability measurements are performed to demonstrate the robust electrical and thermal properties of CNF vias for next-generation on-chip-interconnect designs.**

***Index Terms*—Carbon nanofiber (CNF), interconnect, via.**

I. Introduction

CARBON NANOFIBERS (CNFs) and carbon nanotubes (CNTs) have been investigated as candidate materials to replace or augment the existing copper-based technologies for on-chip interconnects. The basis for these studies is a derivative of their robust thermal [1], electrical [2]–[5], and mechanical [6] properties, in addition to their high-aspect ratio. The need to find alternative interconnect materials is imperative as copper resistivity is rapidly increasing with decreasing linewidth, inevitably causing latency issues due to both line resistance [7], [8] and load capacitance [3]. Perhaps the most troublesome issue with the current state-of-the-art copper interconnects is the reliability concern due to electromigration [9]. In addition, processing difficulties in terms of etching ideal via sidewall profiles and void-free filling of copper will be exacerbated with the decreasing linewidth. Initial electrical characterization results, using carbon-based nanostructures for interconnect applications, have been demonstrated [2], [4], [10], [11], providing encouraging trends for their implementation in next-generation circuit integration schemes. A novel processing paradigm shift, using a bottom-up approach for interconnect fabrication [4], [12], provides a viable alternative to the copper damascene process and can be applied to features in the sub-20-nm regime. Vertically aligned, freestanding CNF arrays [Fig. 1(a)] are embedded in SiO_2 for structural rigidity and electrical isolation. The resulting structure used for the current–voltage ($I-V$) measurements is shown in Fig. 1(b). Fig. 1(c) shows the cross-sectional scanning transmission electron microscope (STEM) image of a single CNF exhibiting the stacked-cone morphology typical of nanofibers grown using our plasma-enhanced chemical vapor deposited (PECVD) process. The alignment of each graphite sheet is not parallel to the nanofiber axis. In contrast, Fig. 1(d) shows a multiwall CNT synthesized by an arc discharge where each graphite sheet is parallel to the tube axis [13]. The morphology and alignment of these graphitic layers define the key difference between CNFs and CNTs. Despite their defective morphology, CNFs exhibit advantages over multiwall CNTs in manufacturability because of lower growth temperatures and superior vertica l alignment. Our recent work demonstrates a significant improvement in the PECVD growth process enabling the growth of CNFs with microstructure approaching multiwalled carbon nanotubes using an optimized catalyst [14]. In Section II, the conduction mechanisms for both CNFs and CNTs are discussed in terms of basal plane (a-axis) and normal to basal plane

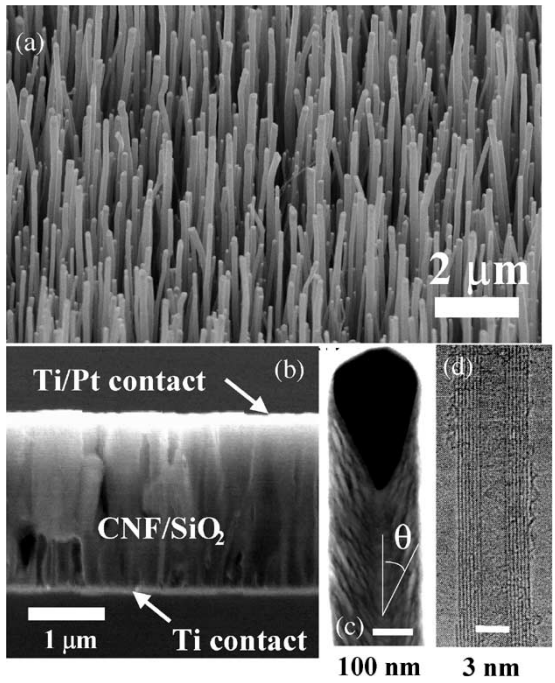

Fig. 1. (a) As-grown vertically aligned CNF array. (b) CNF array embedded in SiO_2 for temperature-dependent measurement. (c) STEM image of single CNF showing stacked-cone morphology. (d) TEM image of single CNT showing well-ordered graphite sheets parallel to the tube axis [13].

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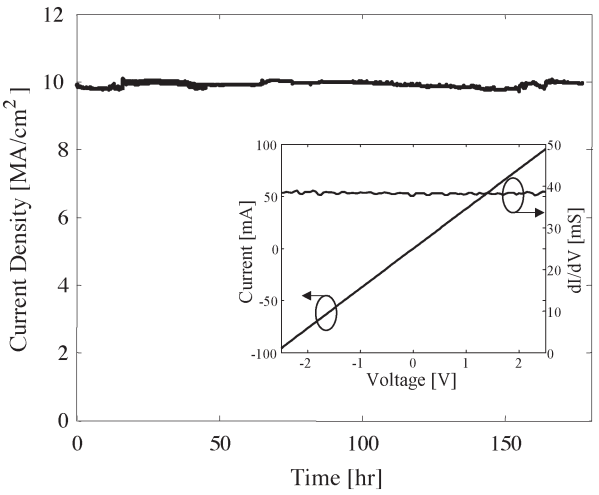

Fig. 2. Room-temperature reliability measurement of CNF via at $J_{\rm ave} = 1 \times 10^7$ A/cm^2. Inset: current and differential conductance versus voltage for the CNF via following 180 h of continuous stress at a constant voltage of 1.5 V.

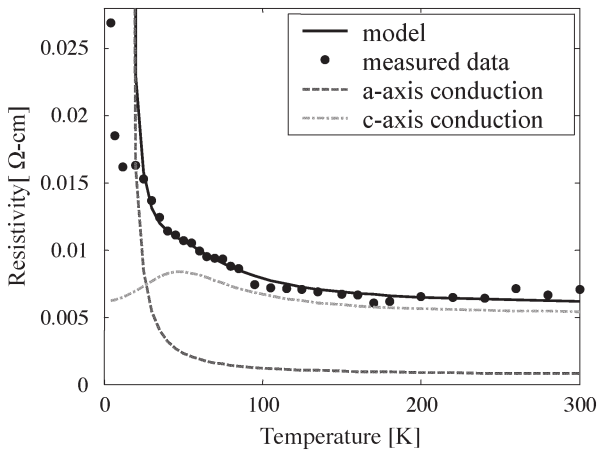

Fig. 3. Resistivity versus temperature for Ni-catalyzed-CNF-array via. Modeling of a-axis and c-axis components of conduction exhibits the dominant electron-conduction mechanism for different temperature regimes. a-axis and c-axis conduction components are from (1).

(c-axis) graphite conduction. The effects of these intrinsic properties on electrical conductance, reliability, and contact resistance are also discussed in this letter. These results provide guidance on how to improve CNF quality and contact interface engineering to approach the desired performance metrics of state-of-the-art copper technology.

II. CNF Vias

The via structures studied here were fabricated using bottom-up techniques described in [4] and [12]. The metal stack used for nickel-catalyzed-CNF growth consists of a thin Ti adhesion layer (30 nm), followed by a 35-nm layer of Ni deposited by ion-beam sputtering. Following PECVD of the CNF array, producing CNFs of 50–100 nm in diameter and 4 μm in length, tetraethylorthosilicate CVD is used to fill the gaps of the interstitial spaces between the individual CNFs with SiO_2 for mechanical stability and electrical isolation [Fig. 1(b)]. Subsequent mechanical polishing leaves CNF tips protruding above the planar SiO_2 surface by approximately 30–50 nm [4]. The exposed tips are metallized with a contact pad (20 nm Ti/40 nm Pt) formed using ion-beam sputtering at an 8-kV accelerating voltage resulting in a 4-μA beam current.

The state-of-the-art copper via technology is susceptible to reliability failures when carrying high current density ($> 10^6$ A/cm^2) due to electromigration. Nanoscale carbon structures are an attractive option to alleviate the electromigration issue, as demonstrated in previous studies [10], [11], [15]. A key metric in measuring the reliability for on-chip interconnects is current-carrying capacity [16]. In this paper, CNF vias are electrically stressed by passing high current density through the via and monitoring the time-depenent electrical characteristics. We demonstrate that CNF vias can exceed the current density goal set by the International Technology Roadmap for Semiconductors (ITRS) for the year 2009 [16] by almost a full order of magnitude. Using current sensing atomic force microscopy (CSAFM) [2], [4], 23 discrete CNFs are determined to be in the 7-μm^2 measured area. At a constant voltage of 1.5 V resulting in an average current of 82 mA, the calculated average current density is 1×10^7 A/cm^2. Fig. 2 shows a negligible change in the current density with time during the 180-h measurement period, demonstrating electrical integrity of both the CNFs and junctions between the nanofibers and metal contacts. The inset of Fig. 2 shows the $I-V$ characteristics of a CNF-array via (under an 18×18 μm contact pad), showing no anomalous behavior following the stress measurement.

The typical resistance measured for a single Ni-catalyzed CNF at room temperature is 13.0 ± 3.0 kΩ for 50-nm diameter CNFs using both CSAFM and a bulk measurement technique [2], approximately 30 times smaller than our original measurements [4] after optimization of CNF synthesis and metal-contact formation. Since a 4-μm-tall via with such small lateral dimensions would not be used in practice, we can expect, based on previous studies [17], that the fiber resistance would be much less for a submicrometer via in sub-45-nm technology nodes.

Novel integration schemes can also be developed to significantly improve the performance. An integration scheme, suitable for carbon-based on-chip interconnects adopted in a recent study, makes use of bundles of small-diameter CNTs in parallel to reduce the overall resistance [11]. One can also make use of parallel conducting channels within multiwall CNTs, as demonstrated in [18], [19]. To understand the intrinsic limit of the conductivity related to the electron transport mechanism, we carried out a series of temperature-dependent resistivity measurements from $\sim$ 4 to 300 K on Ni-catalyzed CNFs. The result obtained from this measurement (Fig. 3) is typical of carbon microfibers that have near-zero bandgaps [20]. However, it deviates from the model presented in [20] because of saturating resistivity at temperatures above 180 K, indicative of a metallike conduction. A plausible explanation is that the resistivity is affected by the CNF microstructure [Fig. 1(c)]. Since the CNF walls are not parallel to the axis, electron conduction cannot take place purely within the basal planes of graphite, as one would expect from a multiwall CNT. In the case of the CNT, one would expect purely an a-axis conduction, facilitating an efficient transport of electrons through the entire tube due to 1-D quantum confinement in the nanotube. The

combination of serial a-axis and c-axis conduction mechanisms contributes to the unique properties of temperature-dependent electron conduction in the CNF array. This behavior is also expected based on the previous studies of CNF electrical characteristics [5], [21]. To model this temperature-dependent behavior, we have combined two previously developed models for both a-axis [22] and c-axis resistivities [23]. Using the data from prior measurements of pure a-axis [24] and c-axis [23] graphite resistivities, the following model is implemented:

$$\rho(T) = \rho_0 + (\rho_a \sin^2\theta)\exp\left(\frac{-E}{kT}\right) + (\rho_c \cos^2\theta)\left(\frac{1}{gT^2 + \frac{b}{T^2+c}}\right) \quad (1)$$

The activation energy (E) is extracted from the measured data in [24], while the fitting parameters g, b, and c are extracted from the data in [23]. The values for the saturation resistivity ρ_0 ($0.0052\ \Omega \cdot$ cm), a-axis resistivity parameter ρ_a ($9.7 \times 10^{-4}\ \Omega \cdot$ cm), c-axis resistivity parameter ρ_c ($4.2 \times 10^{-3}\ \Omega \cdot$ cm), and effective CNF cone angle $\theta(53.6^\circ)$ are treated as fitting parameters for (1). While the values extracted for a-axis and c-axis resistivities are higher than published values [25] by two orders of magnitude due to the defective CNF microstructure, the ratio $\rho_a/\rho_c = 0.23$ is the same for the values extracted from (1) and graphite, thereby validating the model for this study. The effective cone angle extracted is consistent with the high-resolution transmission electron microscopy (TEM) characterization at the CNF base, where the electron conduction occurs primarily normal to the basal plane due to the large cone angle in that region [14].

In addition to using Ni as a catalyst material, Pd as a catalyst is also being explored due to the improved microstructure over Ni-catalyzed nanofibers, thus facilitating more efficient electron conduction [14]. Using a growth stack of Ti/Pt/Ti/Pd (20 nm/300 nm/20 nm/35 nm), CNFs are grown using the same PECVD conditions as the Ni-catalyzed process. The Pd-catalyzed-CNF structures characterized by the CSAFM technique exhibit a significantly lower resistance (9.0 ± 1.6 kΩ) compared to Ni-catalyzed CNFs over many 50-nm-diameter structures measured. The lowest resistance value we have measured, thus far, is 5.8 kΩ for a single 21-nm diameter, 4-μm long Pd-catalyzed CNF, corresponding to a resistivity of 50 $\mu\Omega \cdot$ cm. This result is roughly equivalent to the electrical resistivity measured for basal plane (a-axis) graphite, ranging from 40–80 $\mu\Omega \cdot$ cm [22]. Comparing this to a model [26] scaled down from the current copper-interconnect technology, the CNF result, without future improvements, will not achieve the predicted 312 Ω for the 21-nm diameter 4-μm-tall copper via. Improvements are certainly possible, as mentioned before, in growth processes, material quality, contact interface engineering, and developing novel-processing schemes. It also must be cautioned that the predicted ideal copper resistance is based on the assumption that the material does not undergo any major physical changes at such a small size, such as catastrophic failure due to electromigration, or additional resistance contributed by grain boundary scattering, sidewall roughness scattering, and voids. Scattering mechanisms in small-dimensioned copper wires have been investigated [7], [8], and reliability has recently been the topic of experimental works [9]. The results of these studies lead to the conclusion that resistivity and reliability are the key parameters for downscaling of interconnect structures. The copperlike electromigration failure mode has not been observed for carbon-based structures as demonstrated in this paper and in [11], [15].

III. Conclusion

In this letter, we have demonstrated the utility of CNF vias for on-chip-interconnect applications. The reliability and temperature-dependent conductance characteristics of these CNFs are compared to ITRS technologies for future technology nodes. These results support the viability for implementation of carbon nanostructures in future-generation on-chip-interconnect schemes.

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