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Current Prospects and Challenges in Negative-Capacitance Field-Effect Transistors

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ABSTRACT For decades, the fundamental driving force behind energy-efficient and cost-effective electronic components has been the downward scaling of electronic devices. However, due to approaching the fundamental limits of silicon-based complementary metal-oxide-semiconductor (CMOS) devices, various emerging materials and device structures are considered alternative aspirants, such as negative-capacitance field-effect transistors (NCFETs), for their promising advantages in terms of scaling, speed, and power consumption. In this article, we present a brief overview of the progress made on NCFETs, including theoretical and experimental approaches, a current understanding of NCFET device physics, possible physical mechanisms for NC, and future functionalization prospects. In addition, in the context of recent findings, critical technological difficulties that must be addressed in the NCFET development are also discussed.

INDEX TERMS Negative capacitance, QSNC model, NCFET.

I. INTRODUCTION

After several decades of silicon-based device development, the fundamental limits of silicon technology have given rise to emerging technologies to resolve issues relating to scaling, switching speed, short-channel effect, thermal stress, and power consumption. The operating voltage is lower than 1 V for advanced FinFETs [1]. Lowering the power consumption of the integrated circuits (ICs) is essential to maintain the same ON current while reducing the operating voltage. However, the carrier density described by the Boltzmann distribution implies that a subthreshold swing (SS) lower than 60 mV/dec at room temperature cannot be achieved within the drift-diffusion transport framework. To overcome the limitations of long-standing device physics, new device structures such as tunnel field-effect transistors (TFETs) [2], [3], [4], impact ionization MOSFETs (I-MOSFETs) [5], nanoelectromechanical field-effect transistors (NEMFETs) [6], and negative-capacitance field-effect transistors (NCFETs) [7], [8] have emerged. While TFET utilizes the tunneling current between the degenerately doped source and drain and demonstrates sub-60 mV/dec SS, the low ON-current and the complicated device structure still preclude its application in an IC [9].

On the other hand, NCFET has a device structure similar to FinFET and takes advantage of the voltage amplification effect at the internal node of the ferroelectric/dielectric (FE/DE) stack [10], [11], [12]. The NCFET gate stack uses a series connection of an oxide capacitor (C_{MOS}) and a ferroelectric capacitor (C_{fe}) as an equivalent gate-oxide capacitor, as shown in Fig. 1(a). The term "negative capacitance" (NC)

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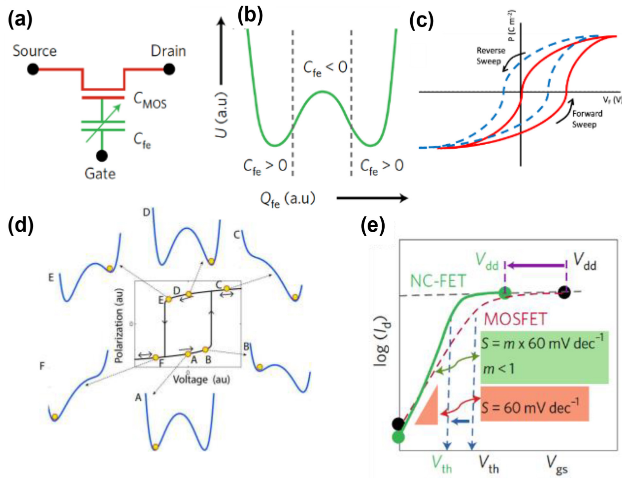

FIGURE 1. (a) Circuit representation of a Negative Capacitance Field Effect Transistor (NCFET). (b) Energy versus charge behavior of a typical NCFET. (c) Schematic illustration of the ferroelectric polarization *P(t)* as a function of the ferroelectric voltage (V_F), (d) Ferroelectric capacitor polarization-voltage hysteresis showing energy landscapes at various positions, and (e) effect of NC performance on the subthreshold slope.

refers to negative differential capacitance resulting from the potential energy (U) versus charge Q_{fe} relationship, $C = [d^2U/dQ_{fe}{}^2]^{-1}$, which reveals a negative value near the local maximum in a ferroelectric material, as shown in Fig. 1(b). The instability of negative capacitance due to the energy barrier can be minimized by connecting an oxide capacitor in series. When an electric field is applied, a typical ferroelectric material shows polarization and hysteresis behavior. The imprint in the ferroelectric material can shift the hysteresis loop, as demonstrated in Fig. 1(c). A ferroelectric material might offer an NC state only in a particular region ($C_{fe} < 0$), as shown in Fig. 1(b). Beyond this region, $C_{fe} > 0$, hysteresis becomes apparent, and the corresponding energy landscape at various positions is shown in Fig. 1(d). The improved performance of an NCFET with lower SS and driving voltage compared to that of a conventional MOSFET is shown in Fig. 1(e). In recent years, the sub-60 mV/dec SS has been observed in many experimental works [13], [14], [15], [16], [17], [18], [19], [20], and the direct measurement of the NC effect has been claimed to validate the NC theory [21]. However, there is much controversy on this subject, as reported by researchers, such as studies on the existence and true genesis of the NC region [22], the origin of the sub-60 mV/dec SS, the validity of the single-domain Landau-Khalatnikov theory for multidomain FE (e.g., HfO_2-based FE materials) [8], among others. Therefore, compiling and assessing these reported analyses will be useful based on the accumulated theoretical arguments and experimental evidence.

In this paper, recent developments in NCFETs are critically reviewed. Typical numerical modeling and the assumptions used are explained for a better understanding of the origin of the NC region. The theoretical studies on the origin of quasi-static negative capacitance (QSNC) and recent experimental works are examined. From a device application perspective, we focus on the reported ultra-steep SS, hysteresis loops and their origin, and the sustained region of the low SS. Furthermore, we discuss the possible mechanisms underlying the observed ultra-steep SS. Finally, we conclude the paper by pointing out the challenges and prospects of NCFETs for practical applications.

II. THE ORIGIN OF NC IN FERROELECTRIC MATERIALS

The NC properties of FE materials have made them a fascinating scientific topic and attractive for versatile device applications [23], [24], [25]. The capacitance C of a device is defined as the fluctuation of its charge Q with respect to its voltage V ($C=dQ/dV$). An increase in charge ($dQ>0$) causes a rise in voltage ($dV>0$) in a conventional capacitor and vice versa. Therefore, an increase in charge ($dQ>0$) in the case of NC leads to a decrease in voltage ($dV<0$) and vice versa. The capacitance C of a parallel-plate capacitor with dielectric material between the plates can be expressed as [26]

$$C = \varepsilon\left(\frac{A}{d}\right) = \varepsilon_0\varepsilon_r\left(\frac{A}{d}\right) = \frac{dD}{dE}\left(\frac{A}{d}\right) \quad (1)$$

where ε_0, A, d, D, and E denote vacuum permittivity, plate area, plate separation, electric displacement field, and electric field, respectively. In the case of a non-linear dielectric medium, the dielectric constant ε_r is a function of the electric field (E), with the displacement field given by $D=\varepsilon_0 E+P$. Negative permittivity ($\varepsilon_0\varepsilon_r= dD/dE<0$) is seen in the case of NC. For linear dielectrics, polarization (P) is a linear function in the same direction as E, resulting in $D=\varepsilon_0\varepsilon_r E$ and a positive ε_r [27]. Because of their non-centrosymmetric crystal structure, FE materials are non-linear. They exhibit polarization even when no electric field is present, a phenomenon known as spontaneous polarization. This spontaneous polarization occurs because dipole moments exist and accumulate in the direction normal to a flat surface, resulting in a net polarization. FE materials have two stable polarization states at the zero electric field, which may be switched by introducing an electric field larger than the coercive field E_c [25], [28]. It is evident from Fig. 2(a) that the central ion in the FE material (lead zirconate titanate or $Pb[Zr_xTi_{1-x}]O_3$ (PZT)) is slightly off-center and may flip between two stable locations. The non-centrosymmetric structure of ferroelectric materials leads to a remanent polarization, as seen in Fig. 2(b).

For FE materials, the permittivity can be expressed as

$$\varepsilon_0\varepsilon_f = \frac{dD}{dE} = \varepsilon_0 + \frac{dP}{dE} \approx \frac{dP}{dE} \quad (2)$$

When polarization occurs in the opposite direction of the applied electric field, with $dP/dE < 0$, the NC state is observed, as shown in Fig. 2(c). The main cause of NC is the instability of FE polarization. The free energy per

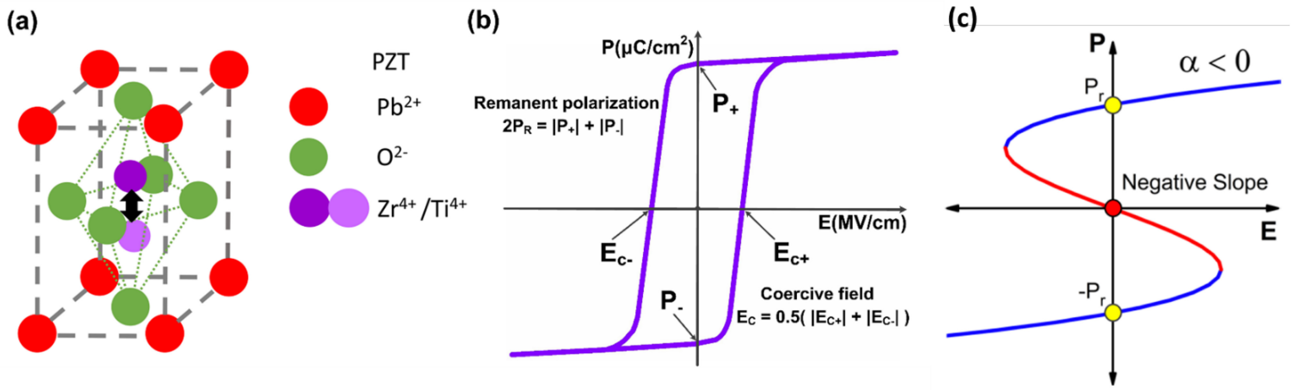

FIGURE 2. (a) Illustration of the two stable locations of a core Zr^{4+} or Ti^{4+} ion in a PZT crystal [23]. (b) A typical ferroelectric hysteresis curve (PE loop), depicting the essential features of remnant polarization and coercive field. (c) Ferroelectric $P(E)$ behavior showing negative slope in the region where P and E are in opposite directions.

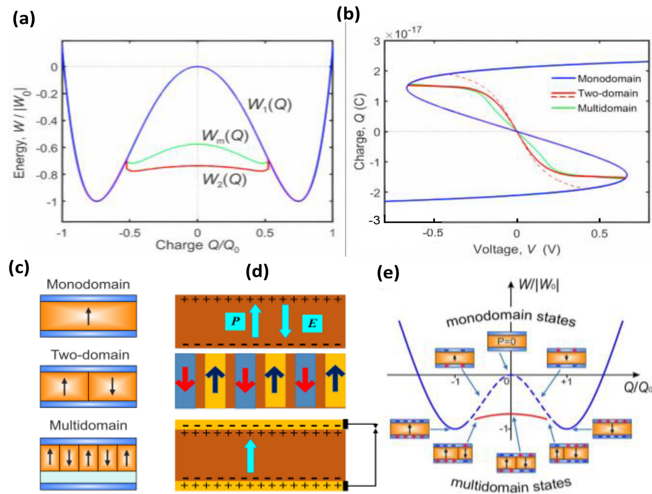

FIGURE 3. (a) The FE free energy vs. applied charge (W-Q) relation. (b) The charge-voltage characteristics (Q-V) are obtained from (a). Blue, red, and green lines represent the monodomain, two-domain and multidomain states, respectively. (c) An illustration of a ferroelectric layer's domain arrangements. Monodomain, two-domain, and multidomain states are shown from top to bottom [30]. (d) FE monodomain samples where polarization (P) and surface charges induce depolarization field (E) are shown. (middle) Formation of the periodic domain structure with the up/down oriented polarization and (bottom) the FE sample with short-circuited electrodes vanishes the depolarization field. As a result, the monodomain structure with uniform polarization is formed again [31]. (e) The normalized energy and polarization states of the ferroelectric (orange) capacitor as a function of the normalized driving charge. The equilibrium charge and energy of the monodomain short-circuited capacitor are represented by Q_0 and W_0, respectively. The dashed line demonstrates the unstable energy of the monodomain state. The red curve depicts the energy of a stable two-domain state [30].

unit volume for FE can be expressed using the Landau model [29].

$$W(P) = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \tag{3}$$

Here, α, β, and γ are Landau coefficients which are anisotropy constants. Below the Curie temperature, $\alpha<0$ and $\beta>0$. The free energy profile for a FE material is displayed in Fig. 3(a). The unstable polarization state occurs at the maximum energy point ($Q = 0$), whereas the two energy minima of the curve correspond to stable states, as seen in Fig. 3(a). By investigating the minima of W with respect to P ($Q=\varepsilon E+P\approx P$, for FE materials), as shown in Figure 3(a), the electric field can be written as

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5. \tag{4}$$

Differentiating E with regard to P yields the reciprocal of permittivity.

$$(\varepsilon_0\varepsilon_f)^{-1} = 2\alpha + 12\beta P^2 + 30\gamma P^4 \tag{5}$$

The permittivity must be negative as $\alpha<0$ at lower values of P, resulting in a negative slope in the "S"-shaped charge-voltage, Q-V, curve (see Fig. 3(b)). The negative permittivity region (i.e., NC) is thermodynamically unstable when only the FE is considered, as illustrated in Fig. 3(a). Therefore, FE materials are usually incorporated into the larger device structure to achieve thermodynamically stable NC states, minimizing the system's total free energy.

Various domain models for the FE layer are demonstrated to describe the NCFET [30], as shown in Fig. 3(c). While the downward curvature at $Q = 0$ is conserved, the energy of the multidomain state is lower than that of the monodomain state, as depicted by the red line in Figures 3(a) and (e). Despite maintaining the NC in a multidomain arrangement, domain creation may have several unintended consequences that make it difficult to realize the NCFET. The conducting channel is particularly vulnerable due to inhomogeneous charge [32] and electric field distribution [33] created by the domain. The transport mechanism can explain how domains form in FE layers.

Figure 3(d) illustrates the depolarization surface charges of $+P_0$ at the top and $-P_0$ at the bottom of the FE layer with uniaxial anisotropy for a monodomain structure. A depolarization electric field, $E = -P_0/\epsilon$, is induced in the FE layer due to charge accumulation on both sides of the FE layer, with the induced field pointing in the opposite direction to the polarization. As seen in the central figure of 3(d), this uniform polarization is disrupted and splits into two alternating

sequences of up and down polarized domains. This type of domain texture was discovered in ferroelectric-dielectric heterostructures [34], [35]. Furthermore, it was discovered that the FE layers have a negative permittivity (i.e., the electrostatic displacement in ferroelectric layers is driven in the opposite direction to the average intrinsic field) [36], [37]. It is hard to use the negative permittivity effect in NC devices because depolarization fields are canceled out when metallic electrodes are placed on the surface of the FE layer, as seen in Figure 3(d). The polarization state of the ferroelectric material can be altered, and negative capacitance can be created by providing an external electric field greater than the coercive field [8].

The FE layer of an NCFET acts as a negative capacitor, amplifying the surface potentials more than the gate voltage. Consequently, the NC effect substantially lowers the SS below the Boltzmann limit. The SS can also be expressed as [8]

$$SS = \frac{\partial V_G}{\partial log_{10}(I_{DS})} = \frac{\partial V_G}{\partial \psi_s} \frac{\partial \psi_s}{\partial log_{10}(I_{DS})} \cong \frac{\partial V_G}{\partial \psi_s} 2.3(kT/q) \tag{6}$$

Here, ψ_s is the surface potential, and the term $\frac{\partial V_G}{\partial \psi_s}$ is defined as the bulk-charge factor (m) which can be expressed as [38]

$$m = \frac{\int_{Q_1}^{Q_2} \left(C_s(Q)^{-1} + C_{ins}(Q)^{-1}\right) dQ}{\int_{Q_1}^{Q_2} C_s(Q)^{-1} dQ} \tag{7}$$

Here, Q is the charge on the gate, Q_1, Q_2 correspond to V_{G1}, V_{G2}, $C_s(Q)$ is the minimum depletion capacitance at the source, and $C_{ins}(Q)$ is the capacitance of the gate insulator, respectively. For a conventional FET with constant C_s and C_{ins}, (7) becomes

$$m = \left(1 + \frac{C_s}{C_{ins}}\right) \tag{8}$$

In conventional FETs, SiO_2 is utilized as a gate insulator that shows positive capacitance ($C_{ins} > 0$), resulting in $m \geq 1$, which makes it impossible to obtain an SS less than 60 mV/dec at 300 K. But in NCFET, $C_{ins} < 0$ with $C_s > 0$ results in m being less than one, which makes it possible to achieve an SS less than 60 mV/dec. The overall gate capacitance, $C_G(Q)^{-1} = C_s(Q)^{-1} + C_{ins}(Q)^{-1}$ [Fig. 4(a)], must be positive to enable hysteresis-free stable functioning of NCFETs [8], [19], [39], which necessitates adherence to the following criteria throughout the NC regime.

$$C_s(Q)^{-1} > -C_{ins}(Q)^{-1} \tag{9}$$

$C_{ins}(Q)$ versus Q and $C_s(Q)$ versus Q characteristics [Fig. 4(b)] aid in comprehending the precise lower limit of SS for NCFETs. The NC gate insulator has distinct operating regimes for positive ($C_{ins}(Q) > 0$) and negative ($C_{ins}(Q) < 0$) capacitance [solid line in Fig. 4(b)]. The border between both regimes occurs at $Q = Q_{c1}$, where $C_{ins}(Q_{c1}) = \infty$ (infinite insulator capacitance), and the NC regime extends from $Q = Q_{c1}$ to $Q = Q_{c2}$. Inversion has a higher $C_s(Q)$

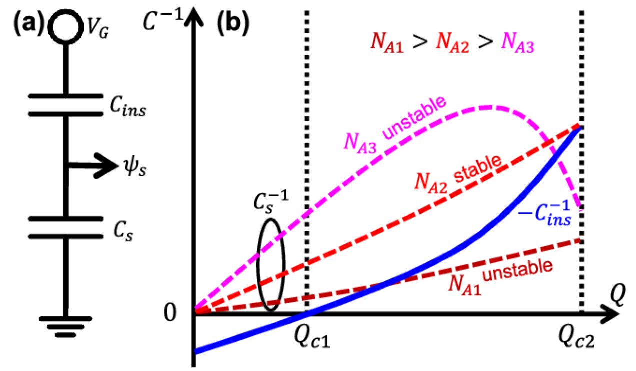

FIGURE 4. (a) Equivalent capacitance model for a conventional FET and (b) generic C_{ins} (Q) - Q (solid line) and C_s (Q) - Q (dotted lines for three different values of N_A) characteristics for NCFET [38].

value than subthreshold, which depends on channel doping N_A [21]. Therefore, $C_s(Q)$ and $-C_{ins}(Q)$ must be tightly matched to find the minimum SS, and to describe it $C_s(Q)$ is shown for three distinct values of N_A in Fig. 4(b). Even at subthreshold, $C_s(Q)$ surpasses $-C_{ins}(Q)$ for N_{A1}, making the gate insulator unstable. For N_{A3}, the channel inverts, and $C_s(Q)$ surpasses $-C_{ins}(Q)$, rendering the gate insulator unstable once more. The channel stays in subthreshold for N_{A2} throughout the NC regime, and a minimal SS is obtained as $C_s(Q)$ and $-C_{ins}(Q)$ are closely matched.

III. THEORETICAL STUDIES OF NCFET

In 2008, Salahuddin and Datta [8] introduced the QSNC theory based on the internal free energy versus polarization relationship reported by Landau-Ginzburg-Devonshire (LGD) [40], which can explain an intrinsic NC region for a FE capacitor, as shown in Fig. 1 (c). The voltage amplification effect arises when the charge changes during the ferroelectric switching of the multidomain at the internal node of the FE/DE stack. The potential benefit of NCFET is to achieve a low operating voltage without sacrificing the ON current. According to the QSNC theory [11], [12], the NC region is stabilized near zero polarization of the FE layer. A voltage smaller than the coercive voltage can be applied during the turn-on operation. This would require a relatively thick FE layer, which adversely limits the overall capacitance of the FE/DE stack. One distinct feature of NCFET is the lack of hysteresis since no switching polarization is involved in stabilizing the NC region, even if NCFET has a device structure similar to ferroelectric FETs (FeFETs). Various combinations of FE and channel materials have been reported to exhibit a sub-thermionic SS (< 60 mV/dec at room temperature) [22], [31], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56]. However, the real origin of the steep SS is rarely analyzed or examined. Many experimental reports do not document whether such steep SS is due to the QSNC stabilization or the transient NC. Cao and Banerjee [12] demonstrated that well-designed cutting-edge FET topologies such as FinFET, SOIFET, carbon nanotube FET, 2D materials-based

FET, and nanowire FET could offer a small trap density, low channel doping, and exceptional electrostatic integrity. However, these devices receive very little benefit from NC in achieving sub-thermionic SS due to their negligible parasitic capacitance compared to gate capacitance. This study showed that quantum capacitance (QC) is the major bottleneck to attaining hysteresis-free sub-thermionic SS. Thus, FETs that can operate under the QC limit are preferable for developing NCFETs. In this regard, Yang et al. [57] recently reported both theoretically and experimentally a 2D-materials-based negative QC FET (NQCFET) with steep-slope switching capability. They showed that mono-layer graphene encapsulated in the gate stack of a MoS_2 FET provides a negative QC based on the electron-electron interactions by adjusting the Fermi energy near the Dirac point. With only a minimal hysteresis (∼10 mV), they obtained a minimum SS of 31 mV/dec. We will now discuss some representative NCFET results that support the QSNC hypothesis. As explained above, the focus is not limited to the reported SS values but includes the possible origins of the SS and a practical application-oriented perspective. Because of internal voltage amplification and voltage pinning effects, Guha and Pachal [58] obtained an average SS of 27 mV/dec and a high I_{ON}/I_{OFF} of 10^{16} in their theoretical study. Furthermore, the integration of FE materials (NC effect) in the gate stack of tunnel FETs provides a steeper off-to-on transition and an outstanding on-off current ratio, making these NC-TFETs suitable for low power consumption applications, as shown in their study [2], [3], [31], [56], [58].

Even though the studies mentioned above support the QSNC theory, Liu et al. [59], [60] reported reverse switching at the falling edge during the pulse measurement with the hysteresis-free NC effect by numerical simulation using the nucleation limited switching (NLS) model, which provides an alternative explanation of NC effects without invoking the QSNC theory. Even though QSNC theory supports the presence of sub-60 mV/dec SS in NCFETs at sufficiently high voltages, Liu et al. observed the NC effect in FE capacitors without charge injection by using the NLS model [59], [60]. As Kittl et al. [61] pointed out, the total energy of the two capacitors connected in series (FE/metal/DE structure) is expressed as a function of the free charge. The free energy of the FE layer adopts the same Landau's phenomenological theory, which uses polarization as the parameter. If the free energy is expressed as a function of the free charge, the second derivative of the energy with respect to the free charge is always positive, and no NC region is physically in the model. In terms of another commonly used FE/DE stack, the total free energy of the bilayer dielectric is expressed as the sum of the two layers using polarization as the parameter. In the QSNC theory, one assumption often quoted is the constant polarization in the DE and FE layers ($P_{DE} = P_{FE} = P$). The total energy minimum is obtained around $P = 0$ if the capacitance matching condition is satisfied. However, a polarization discontinuity (ΔP) usually results in net interfacial charges.

The DE and FE layers can adopt their optimal polarization in many cases. On the other hand, if there is a strong polarization coupling between the two layers, and further considering the energy contribution due to the coupling, both the FE and DE have positive capacitance with similar permittivity. As a result, the total capacitance is larger than the DE layer, but no NC region is involved in the FE layer. In that case, an ultra-small equivalent oxide thickness (EOT) could be obtained, but the sub-60 mV/dec SS is not obtained. On the other hand, the QSNC relies on the region between the two stabilized polarizations above the coercive voltage, which leads to a small range of applied voltages and a limited sustained sub-60 mV/dec region.

Thus far, many theoretical studies based on the QSNC theory have been conducted, including intensive numerical simulations [2], [3], [31], [56], [62], [63] and complex analytical modeling [4], [64], [65]. To understand the operation of NCFETs, some of these theoretical studies considered the total FET gate capacitance to be a constant [8], [66], i.e., these investigations ignored the bias-dependent depletion capacitance. Moreover, the complexity of analytical modeling [4], [64], [65] proposed for the specific NCFETs such as NC-FinFET and NC-2DFET somewhat obscured the design principles, fundamental device physics, and major challenges of NCFETs. These studies also make evident that the precise nature of the NC state is still being debated, i.e., does the NC effect reflect a stable third polarization state or a transient switching effect? Furthermore, the Landau model for steady-state behavior under equilibrium conditions is used to infer the free energy versus polarization relationship. However, using a steady-state model, it is intrinsically difficult to represent switching behavior.

IV. EXPERIMENTAL FINDINGS

A. FABRICATED NCFET DEVICE STRUCTURES

Many of the reported NCFETs have a structure similar to the FeFET, which can be used as a single cell for non-volatile memory. The simplest form uses the FE layer as the gate DE, a metal-ferroelectric-semiconductor (MFS) structure. In this case, the depletion capacitance provides the matching capacitance, which also depends on the gate voltage (thus surface potential). The same gate dielectric stack can be easily applied to other low-dimensional channel materials, including one-dimensional carbon nanotubes and two-dimensional semiconductors (WSe_2, MoS_2, etc.). The main difference introduced by these low-dimensional channel materials is the limited capacitance variation of the channel material, which may help to obtain a steep-slope FET in a wide current range if the capacitance is well-matched with the FE capacitor.

B. NCFET DEVICE PERFORMANCE

Rusu et al. reported the first experimental demonstration of a sub-60 mV/dec NCFET by adopting a polymer FE P(VDF-TrFE)/AlSi metal/SiO_2 as the gate dielectric [67]. A bulk n-type silicon well is used as the channel material to

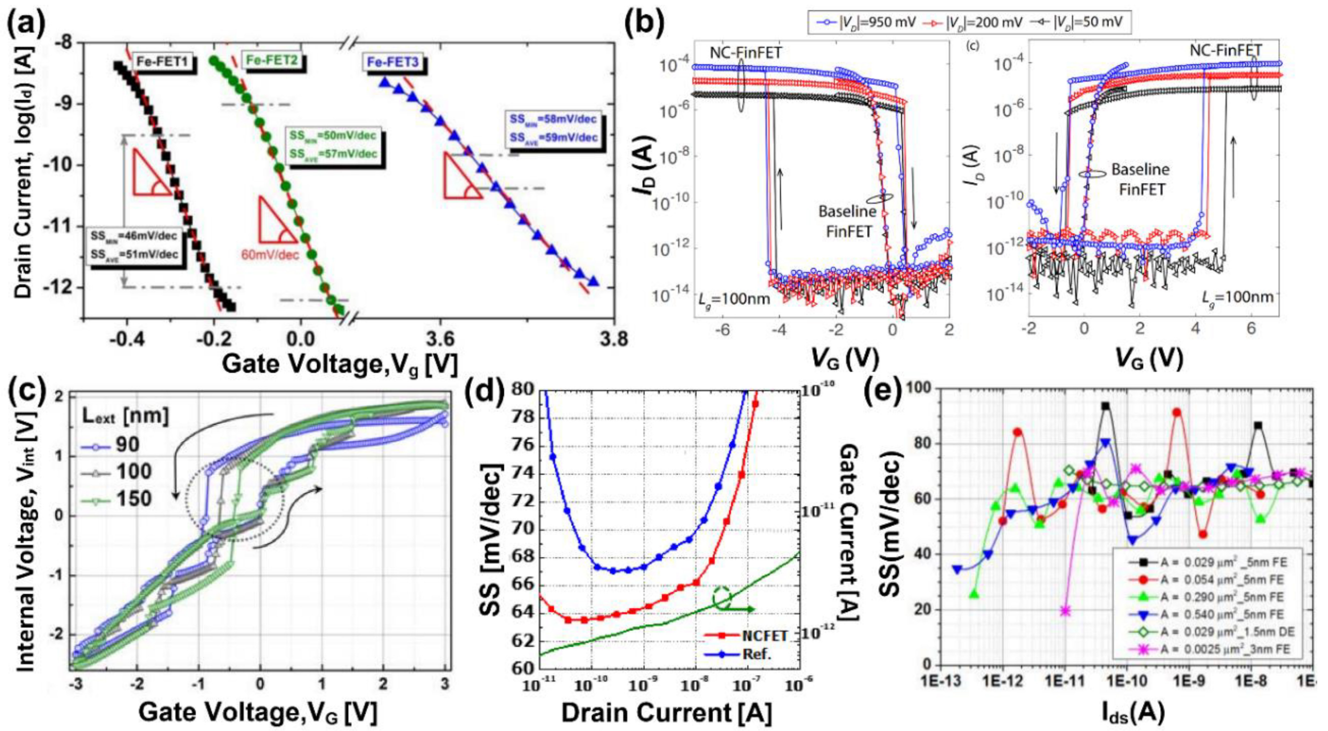

FIGURE 5. (a) $I_d - V_g$ data showing the current range for which SS is smaller than 60mV/dec at room temperature [67]. (b) Comparison of $I_d - V_g$ characteristics of the baseline FinFET and the corresponding p-channel (left) and n-channel NC-FinFET at different drain voltages [69]. (c) Measured internal voltage (V_{int}) versus the gate voltage (V_G) for various source/drain extension lengths, L_{ext} [70], (d) SS/I_g as a function of I_d for L_g=150 nm NC and reference FETs, where L_g is the gate length [17]. (e) Variation of SS in the subthreshold regime for various transistor areas [71].

fabricate a p-MOSFET. An average SS of 51 to 59 mV/dec was observed, and they claimed the internal surface potential is amplified when the FE enters the S-shape of the *P(E)* curve. Furthermore, the minor S shape in the hysteresis loop appears near the FE layer's coercive voltage, contrary to the original QSNC theory [11], [12]. Although it is not specified at the early stage of the study, this phenomenon could be related to the mismatch of the charging rate of the free charge on the metal plate and the switching polarization charges in the FE layer. The hysteresis, the significant variation of the SS value, and the maximum surface potential gain near the coercive voltage suggest polarization switching as the primary origin of the steep SS.

In practical applications, the sub-60 mV/dec region is limited to drain current from $\sim$ pA to $\sim$ nA (Fig. 5(a)), which cannot be used to obtain a low operating voltage device. Furthermore, if we are targeting a low operating voltage, which means a low threshold voltage and an ON current comparable to that of the state-of-the-art Si FETs, a realistic figure of merit (FOM) for the sub-60 mV/dec devices should also consider the current range in the steep-slope region. One can define I_{60} as the drain current above which the SS is larger than 60 mV/dec. This FOM can also be used to compare steep-SS devices, including NCFETs, TFETs, impact ionization FETs, etc. [43]. I_{60} should reach at least 1-10 μA/μm or as close to the ON current for a low operating voltage FET. Jo and Shin. connected an Au/P(VDF-TrFE)/TiN capacitor with a p-channel bulk Si MOSFET and observed SS values < 60 mV/dec in the current range of 10 pA/μm to 10 nA/μm [68]. The capacitance of the FE layer is about 49 pF $\sim$ 52 pF, while the MOS capacitor has a capacitance of 27 fF $\sim$ 47 fF, which is three orders of magnitude lower. With such a configuration, they reported a SS of 48 mV/dec over three orders of magnitude of drain current, which is much better than the same device (110 mV/dec) without the FE capacitor. The hysteresis-free transfer curves could be obtained by limiting the drain voltage while sacrificing the SS, which indicates the importance of FE switching for ultra-steep SS FETs.

Early demonstrations typically used a reasonably long channel length to verify the existence of the NC effect. Researchers have recently attempted to merge the FE capacitor with conventional CMOS transistors, including FinFET and FDSOI structures [53]. In this context, FinFET has emerged as one of the best choices for achieving enough gate control over the channel owing to its superior performance in the subthreshold region [72], [73], [74]. The NC-FinFET, a hybrid structure of the FinFET and the NC state, was introduced in 2015 and validated experimentally to have an SS of 55 mV/dec [75]. NC-FinFETs offer several advantages over other structures, including ease of manufacture, process integration, enhanced current driving capabilities, and the ability to adjust short-channel effects (SCEs) [69], [70], [76], [77], [78], [79], [80], [81]. Prior investigations introduced

two primary architectures to support the NC-FinFETs: Metal–FE–Metal–Insulator–Semiconductor (MFMIS) and Metal–FE–Insulator–Semiconductor (MFIS) structures. The existence of an internal metal gate in the MFMIS structure is the primary distinction between these two architectures. Since the MFM capacitor and the MISFET may be produced separately, MFMIS designs have been used more in NCFET research. In addition, the MFMIS structure gives a greater ON current for FE with large remanent polarization values and reduces hysteresis in the device. In modern CMOS technologies with channel lengths less than 20 nm, the internal metal gate cannot occupy the gate trench and enables charge injection and buildup, limiting NCFET operation even more. The multiple-domain Landau framework is modified to show that the presence of a floating metal gate allows for FE leakage. This leads to NC instability and traps, resulting in threshold fluctuations [46]. A surface potential-based model for an MFIS-type gate-all-around (GAA) NCFET validates this claim. Even though designing both the FE and semiconductor channel individually is impossible [82], [83], [84], MFIS-based FET is the preferred option.

Despite being the most promising candidates for NC applications, the MFS and MFIS gate stacks can hardly be used in the actual construction of the NCFET [26]. The primary challenge is the compulsory production of the nonuniform domain texture caused by the destabilizing influence of the depolarization fields, which are formed by the depolarization charges produced at the FE-Insulator (FI) and FE-Semiconductor (FS) interfaces. Even though the domain structure retains the collective NC effect [37], two significant offshoots prevent its use in the MFS and MFIS FET. These are: (i) the nonuniform field distribution interferes with the creation of conducting channels near the FS interface, and (ii) the high absolute value of the NC cannot appropriately match the depletion capacitance. Furthermore, creating antiparallel domains inside the MFM capacitor would cause the NC to become unstable. However, Luk'yanchuk et al. [85] showed that the two-domain arrangement of the MFM structure offers a stable and operable NC due to the potential of modifying the domain wall by the applied charges, which was not taken into account by Hoffmann et al. [66]. Furthermore, by connecting the MFM capacitor in parallel with the dielectric capacitor, Luk'yanchuk demonstrated that the MFMIS architecture not only mitigated the issues outlined above but also yielded vastly improved MFMIS FET characteristics.

The first structure of NC-FinFET used a $Hf_{0.42}Zr_{0.58}O_2$ FE layer on the MFMIS gate stack, exhibiting an SS as low as 55 mV/dec at $V_D = 0.1$ V, which also decreases with increased annealing temperature [75]. The NC-FinFET with $Pb(Zr_{0.2}Ti_{0.8})O_3$ on the MFMIS gate structure was shown experimentally by Ko et al. [70] with an SS of 20 mV/dec, a hysteresis window of 0.48 V, and $I_{ON}/I_{OFF} = 10^7$. According to this study, the hysteresis window in the NC-FET narrows as the source/drain extension length is extended. Khan et al. connected a short-channel FinFET with an external epitaxial single-crystalline $BiFeO_3$ ferroelectric capacitor [69]. In this work, the size of the FE capacitor (25 μm in diameter) was about three orders of magnitude higher than that of the gate dielectric HfO_2, which might be helpful for capacitance matching. A very small SS of $\sim$ 8.5-40 mV/dec was obtained over eight orders of the drain current, which seems promising. However, a counterclockwise (clockwise) hysteresis was observed for the n-channel (p-channel) FinFET (Fig. 5(b)), which is a typical sign of ferroelectric switching at the coercive voltage. In other words, the device exhibited the typical characteristics of a FeFET. The steep turn-on and turn-off characteristics were obtained near the coercive voltage, which limits its application for low-operation voltage devices. The large hysteresis window of the NC-FET is comparable with the original FE capacitor, indicating that the steep-slope SS is due to the transient switching effect but not NC region stabilization. To decrease the hysteresis window, Ko et al. optimized the FinFET geometry by extending the source/drain extension length for improved capacitance matching [70]. A 60 nm $Pb(Zr_{0.2}Ti_{0.8})O_3$ deposited by PLD was adopted as the externally connected capacitor. The short-channel (70 nm gate length) n-type FinFET exhibited a sub-20 mV/dec SS with a high ON current of $\sim$1 mA. However, a similar counterclockwise hysteresis was observed for n-channel FinFET. The noted stepped internal voltage jump occurred in partial domain switching of the FE layer (Figure 5(c)), suggesting the multidomain property of the FE layer.

To demonstrate the scaling potential of the CMOS- compatible HfO_2-based FE layer for steep-slope transistors, Kwon et al. demonstrated an NCFET with a 1.8 nm Zr-doped HfO_2 (HZO) FE layer integrated with a standard FDSOI substrate [17]. Here, a 2 nm SiO_2 film was thermally grown on top of the silicon before the deposition of the FE layer. The resulting NCFET exhibited an SS $\sim$ 63 mV/dec compared to 67 mV/dec for the FETs with HfO_2 high-k gate dielectric gated FETs. The authors claimed that the NC region of the FE layer was obtained when the silicon channel was depleted, which resulted in a steep-slope subthreshold region of the transistor. When the silicon substrate was in accumulation, the stack emerged from the NC region and entered the stable region as the total charges (polarization) were enhanced. This phenomenon limits the achievable sustained charge amplification range in the sub-thermionic region. They reported that the SS increased as the channel length decreased and was above 110 mV/dec for a channel length of 30 nm. While the FE/DE stack can improve the overall performance of the Si FETs, the lack of sub-thermionic SS provides strong support for the NC stabilization theory (see Fig. 5(d)). Krivokapic et al. [71] demonstrated the improvement of SS (54 mV/dec) for 14 nm FinFET using Si-doped HfO_2 as the FE layer. The SS below the threshold voltage varies considerably due to the multigrain polycrystalline property of the FE layer (see Fig. 5(e)). With various FE/DE stacks, the sub-60 mV/dec characteristics were observed only for some devices, and a constant sub-60 mV/dec was not obtained above $\sim$10 nA

drain current. They also demonstrated ring oscillators based on the FE/DE gated FETs that can operate at the same frequency but with reduced active power. McGuire et al. [86] pointed out that the variable capacitance of the bulk semiconductor during the switching (depletion to inversion) limited the extent of the sub-60 mV/dec region.

Although some recent experiments have confirmed the existence of a metastable NC state in the FE layer [87], [88], [89], [90], [91], the advancement of real devices that are actually useful and focus on NC seems to have been slow. Various characteristics have been seen in experimental demonstrations that are inconsistent with the predictions of current theoretical models. Two primary lines of inquiry must be explored simultaneously if negative capacitance electronics are to move forward. First, a deeper comprehension of the various domain wall configurations crucial for modeling negative capacitance is needed since depolarization often results in the development of domains. The basic idea of the NC comes from the single-domain structure; the impact of the multidomain cannot be neglected in practical devices. Second, by connecting a dielectric capacitor in series with such a ferroelectric material, a considerable amount of charge is forced across the dielectric, dangerously close to breakdown. It is challenging to obtain a sufficient overall increase in the surface potential from the external gate voltage in the subthreshold region since the semiconductor offers a tiny capacitance and delivers substantial negative feedback to the ferroelectric. Therefore, attaining sub-60 mV/decade operation at subthreshold in such a configuration may be challenging. Further, to respond to this negative feedback in the ferroelectric, the capacitance of the semiconductor greatly increases while the transistor is in inversion. As a result, the charge on this device may ramp up the threshold voltage at a faster rate than in a traditional MOSFET, resulting in a lower net supply voltage in the transistor.

C. POSSIBLE ORIGINS OF STEEP SS

The unstable NC region precludes the direct observation of the NC effect in a single FE capacitor. The NCFET provides an indirect way to prove the NC theory through SS reduction. Still, the true origin of SS reduction is a subject of debate because of the complex structure and multiple interfaces in an actual FET device. In the original QSNC theory, the single-domain assumption is essential as the NC region operates near zero polarization. For a multidomain thin film which is more realistic in an actual device, a total zero polarization could be obtained if it consists of equal areas of up and down polarized domains. The negative slope in the $P(E)$ loop without entering the NC region is theoretically investigated on a single FE capacitor by incorporating the depolarization and stray fields due to the multidomain structure [92]. First-principles nonequilibrium molecular dynamics simulations indicate that the negative slope originates from the partial screening of the polarization and is more likely to occur when a significant electric field is applied to the FE layer [93]. By introducing the term internal electric field, E_{int}, which is the applied electric field, E_{app}, subtracting the depolarization field, the negative slope is obtained in the $P(E_{int})$ curves but does not appear in the $P(E_{app})$ curves (Fig. 6(a)).

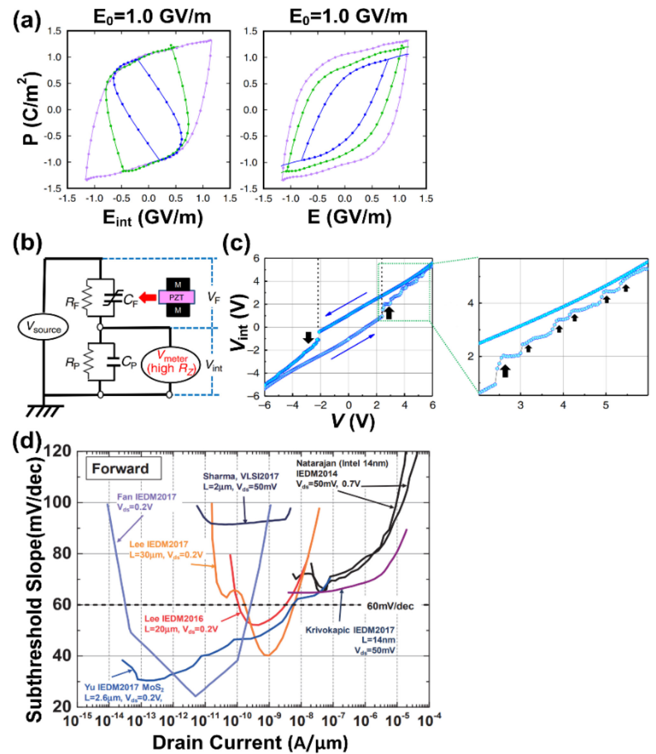

FIGURE 6. (a) Dependence of the polarization on the internal field and applied field in the $PbTiO_3$ film [93]. (b) Equivalent circuit of V_{int} measurement in FE/DE system. R_F and R_P are the insulating resistance of the FE- and DE capacitors, respectively. Note that a high impedance system is required to obtain the accurate V_{int} [94]. (c) V_{int}-V characteristics during V sweeping of FE/DE system, V_{int} jump occur along with V_F drop at $V_F = \sim \pm V_C$ [94]. (d) Benchmark of SS values of some reported NC FETs [84].

Most recently, Li et al. reported a stepwise internal potential-jump phenomenon in measuring the DC voltage applied to the capacitor in a series connection with a metal/PZT/metal FE capacitor [94]. They claimed that the accuracy of their measurement setup is optimized by increasing the equivalent resistance of the voltmeter (Fig. 6(b)). A voltage jump on the paraelectric (PE) layer is observed when the voltage applied to the FE layer approaches the coercive voltage of the FE PZT thin film (Fig. 6(c)), and they attribute the stepwise characteristics to the distribution of the coercive voltage of the domains in the multidomain PZT layer. The ultra-steep SS < 60 mV/dec is also obtained by connecting a PZT capacitor with a standard Si transistor with a SiO_2 gate dielectric. With this model, the low SS is obtained near the coercive voltage, which means a low-voltage and hysteresis-free device is probably not obtained with the metal/FE/metal/DE gate stack. Figure 6(d) shows the reported SS versus drain current from various authors, which reveals that the I_{60} is limited for the NCFETs [84].

TABLE 1. Summary of achievements and remaining challenges for NCFETs.

Study	Approaches and Findings	Outcomes and challenges
Theoretical [60]	Nucleation-Limited Switching (NLS) model: a hysteresis-free NC effect	Still debating the NLS model and contradicts the QSNC effect and need to modify the assumptions
Experimental [59]	$Hf_{0.5}Zr_{0.5}O_2$ (HZO)-based ferroelectric capacitor: verify the QSNC theory	The observed results contradict four fundamental predictions of the QSNC hypothesis
Theoretical [53]	Combining the FE capacitor with standard CMOS transistors, SOI and double gate (DG) 2D NCFET structures	SOI 2D NCFET agrees with the QSNC theory but steep SS is challenging to obtain for intrinsic DG NCFETs
Experimental [67]	Organic P(VDF-TrFE)/AlSi metal/SiO_2 NC-FET: a sub-60 mV/dec. of SS	Confirm the QSNC theory of internal voltage amplification
Experimental [17]	The NCFET with a 1.8 nm Zr-doped HfO_2 FE layer on FDSOI, 20 mV/dec. of SS	NCFETs at scaled channel lengths
Experimental [71]	Si-doped hafnia FE layer is integrated with the 14 nm FinFET technology	Consistent with the LK model for polycrystalline FE and the SS below the threshold voltage varies
Experimental [86]	2D MoS_2 channel with FE P(VDF-TrFE): 11.7 mV/dec. of SS at room temperture	A steep SS behavior verifying the QSNC theory; instability of the P(VDF-TrFE) FE layer
Experimental [98]	2D MoS_2 channel FET with HZO/TiN/HfO_2 : SS of 8.03 mV/dec	Consistent with the QSNC theory; a clear hysteresis window, not stabilized NC region
Experimental [99]	2D MoS_2 with $Hf_{0.5}Zr_{0.5}O_2$ FE layer and Al_2O_3 capping dielectric layer	The QSNC hypothesis is clearly confirmed. Small SS only sustains at a low drain current <10 nA
Experimental [100]	WSe_2 with a $Hf_{0.5}Zr_{0.5}O_2$/Al_2O_3/Ni/HfO_2: minimum SS of 14.4 mV/dec	The NC effect is confirmed by both the low SS and the negative DIBL
Experimental [101]	MoS_2 FET with an organic FE P(VDF-TrFE): minimum SS of 21mV/dec	Agrees with the QSNC theory, but a very large hysteresis due to the ferroelectric switching
Experimental [102]	FE $CuInP_2S_6$ and MoS_2 channel material: sub-60 mV/dec. of SS	Consistent with the steady-state LK model, the unstable NC region dominates the steep SS
Experimental [103]	CNT and FE/metal/DE: 10 nm 7% Al:HfO_x as the FE layer: 55 mV/dec. of SS	Consistent with the QSNC theory and explore negative capacitance effects with CNTs
Theoretical [104]	The prospect of enhanced surface potential in QSNC theory was re-evaluated	The multidomain ferroelectricity was contrary to the single-domain state in QSNC theory
Theoretical/ experimental [105]	LK and Maxwell's equations: the FE capacitance is substantially non-linear and time-dependent	The steep SS in NCFET demonstrated by the non-linearity of the positive capacitance of FE materials
Theoretical/ experimental [106]	LK and Poisson equations: nonequilibrium Green's function for comprehensive quantum-transport simulations	Consistent with the QSNC theory: need to resolve technical issues such as the influence of process variability.

Further, Su et al. [95] demonstrated that the dynamic behaviors of FE and sweeping voltage significantly influenced the SS and the drain current range. Utilizing the domain switching dynamics of FE [96], they explained that a higher remanent polarization is advantageous for a steeper SS with a wider range of drain currents. Their simulation results showed that the drain current range could only be increased for steeper switching in NCFETs within a restricted region of sweeping rate and FE switching time. Migita et al. [97] showed for the MFMIS structure that the polarization reversal of FE was the genesis of the steep SS. Therefore, choosing a FE with a low *k*-value and low polarization and using thin DE layers would yield a steeper SS. On the other hand, Wang et al. [96] explained that a steeper SS necessitated a greater rate of polarization change ($\partial P/\partial t$) over time. However, optimizing hysteresis and SS simultaneously is not achievable since raising $\partial P/\partial t$ also raises the voltage across the ferroelectric and vice versa. As a result, SS and hysteresis conflict in practical devices.

V. PROSPECTS OF NCFETS

After the publication of Salahuddin and Datta [8], NCFETs have attracted significant attention due to the strong demands of low-power FET technology. Although notable

progress in demonstrating the NC effects theoretically and experimentally, many challenges remain to bring NCFETs to commercialization. For example, realizing stable static NC in the non-transient and non-hysteretic regime remains a daunting challenge. And it needs to be clarified how the NC's fundamental origin related to the formation of the domain state can be properly utilized to implement the NCFET. Table 1 lists the approaches and the critical technological challenges that need to be addressed in the development of NCFETs.

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DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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